FPGA implementation of the complex division in digital predistortion linearizer

ABSTRACT

Since division is not a standard operation for DSP processors and because it can be implemented in several different ways, there is no specific algorithm clearly to choose. It all depends on the requirements, such as accuracy, size and speed. A few suitable algorithms should be selected and implemented in VHDL for evaluation. The implementation is expected to be a part of an existing baseband processor and should be able to handle the high speed requirements while keeping the size down. Here we implement complex division based on Newton Raphson method. This divider will be used in the Digital Predistortion for adaptation of the power amplifiers. Based on the requirements of the input signal, the divider that is implemented here has different features and makes it suitable for digital communication where we deal with complex values. The results of simulation show improvement in hardware resources as compare to other methods.

Keyword: Division; DSP; VHDL; Digital predistortion